Amendments to the Claims:

1-30 (Cancelled)

31. (New) A semiconductor package comprising:

a die pad having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads extending at least partially about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first and second surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion;

a semiconductor chip attached to the first surface of the die pad and electrically connected to at least one of the leads; and

a package body at least partially encapsulating the semiconductor chip, the die pad, and the leads such that the inner lead portion of each of the leads is within the package body and the outer lead portion of each of the leads extends out of the package body.

32. (New) The semiconductor package of Claim 31 wherein the inner end surface of each of the leads and portions of the first and side surfaces of each of the leads which extend along the inner lead portion thereof are covered by the package body.

33. (New) The semiconductor package of Claim 32 wherein:

the package body has opposed, generally planar first and second surfaces; and

a portion of the second surface of each of the leads which extends along the inner lead portion thereof is exposed in and substantially flush with the second surface of the package body.

34. (New) The semiconductor package of Claim 33 wherein the first and side surfaces of the die paddle are covered by the package body.

35. (New) The semiconductor package of Claim 34 wherein the second surface of the die paddle is exposed in and substantially flush with the second surface of the package body.

36. (New) The semiconductor package of Claim 31 wherein the semiconductor chip is electrically connected to the first surface of at least one of the leads via a conductive wire which is encapsulated by the package body.

37. (New) The semiconductor package of Claim 31 wherein:

the semiconductor chip includes an active surface having a plurality of conductive bond pads thereon;

a portion of the active surface of the semiconductor chip is attached to the first surface of the die pad;

the semiconductor chip and the leads are sized and oriented relative to each other such that each of the bond pads of the semiconductor chip at least partially overlaps the first surface of a respective one of the leads; and

each of the bond pads of the semiconductor chip is electrically connected to the first surface of a respective one of the leads.

38. (New) The semiconductor package of Claim 31 wherein:

each of the leads includes an undercut region which is disposed in the second surface thereof and extends to the inner end surface thereof; and

the undercut region of each of the leads is covered by the package body.

39. (New) The semiconductor package of Claim 38 wherein:

the die pad includes an undercut region which is disposed in the second surface thereof and extends to the side surfaces thereof; and

the undercut region of the die pad is covered by the package body.

40. (New) The semiconductor package of Claim 31 further in combination with a second semiconductor chip attached to the semiconductor chip and electrically connected to at least one of the leads, the second semiconductor chip being covered by the package body.

41. (New) A semiconductor package comprising:

a die pad having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads extending at least partially about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first and second surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion;

a package body at least partially encapsulating the die pad and the leads such that the first surface of the die pad and a portion of the first surface of each of the leads extending along the inner lead portion thereof are exposed in a cavity defined by the package body, and the outer lead portion of each of the leads extends out of the package body; and

a semiconductor chip disposed within the cavity and attached to the first surface of the die pad, the semiconductor chip being electrically connected to at least one of the leads.

42. (New) The semiconductor package of Claim 41 wherein the inner end surface of each of the leads and portions of the side surfaces of each of the leads which extend along the inner lead portion thereof are covered by the package body.

43. (New) The semiconductor package of Claim 42 wherein:

the package body has a generally planar second surface; and

a portion of the second surface of each of the leads which extends along the inner lead portion thereof is exposed in and substantially flush with the second surface of the package body.

44. (New) The semiconductor package of Claim 43 wherein the first and side surfaces of the die paddle are covered by the package body.

45. (New) The semiconductor package of Claim 44 wherein the second surface of the die paddle is exposed in and substantially flush with the second surface of the package body.

46. (New) The semiconductor package of Claim 41 wherein the semiconductor chip is electrically connected to the first surface of at least one of the leads via a conductive wire which is disposed within the cavity of the package body.

47. (New) The semiconductor package of Claim 31 further in combination with a lid attached to the package body and enclosing the cavity thereof.

48. (New) A semiconductor package, comprising:

a substrate having opposed first and second surfaces;

a die pad disposed on the first surface of the substrate;

a plurality of circuit patterns disposed on the first surface of the substrate and extending at least partially about the die pad in spaced relation thereto, each of the circuit patterns having an inner end portion and an outer end portion;

a semiconductor chip attached to the die pad and electrically connected to at least one of the circuit patterns; and

a package body at least partially encapsulating the semiconductor chip, the substrate and the circuit patterns such that the inner end portion of each of the circuit patterns is covered by the package body and the outer end portion of each of the circuit patterns is exposed outside of the package body to serve as an input/output terminal.

49. (New) The semiconductor package of Claim 48 wherein the substrate includes a plurality of input/output terminals which are disposed on the second surface thereof and electrically connected to respective ones of the circuit patterns.

50. (New) The semiconductor package of Claim 48 wherein the semiconductor chip is electrically connected to the inner end portion of at least one of the circuit patterns via a conductive wire which is encapsulated by the package body.